ABSTRACT OF THE DISCLOSURE

An input/output circuit includes a reference clock generator configured to generate a reference clock. A signal transmitter is configured to transmit serial data in synchronization with one of the reference clock and a test clock. A signal-receiving circuit is configured to receive the serial data, and to generate a converted signal from the serial data. A test circuit is configured to detect an error between each phase of the converted signal and the test clock when the signal transmitter operates in synchronization with the test clock.